AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

Claim 1. (currently amended) A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for providing data to an output port, comprising:

a memory having a plurality of storage elements, each storage element being adapted to store a bit and provide the bit as an output of said memory ~~having an input and an output, said input being programmably connectable to either a state machine, mircroprocessor, or other programmably controllable data source for selection of data for storage therein~~;

a first multiplexer having a multiplexer ~~an~~ output, having a plurality of inputs receiving the outputs of said memory, and having a control input for selecting, in response to a control signal, an input for connection to said multiplexer output;

a control signal generator connected to the control input of the first multiplexer for generating a control signal to control said first multiplexer to select said first multiplexer inputs for connection to said first multiplexer output; and

a clock edge selector circuit connected to said first multiplexer for providing, in response to an edge select signal, the output of said first multiplexer to said output port selectably on either said rising edges or said falling edges of said clock signal.

Claim 2. (currently amended) The state machine input/output circuit of Claim 1, wherein said clock edge selector circuit, wherein ~~further comprises~~:

the inputs ~~input~~ of the first and second flip-flops are connected ~~coupled~~ to the output of said multiplexer, said first flip-flop changing states on said rising

edge of clock pulse and said second flip-flop changing states on said falling edge of clock pulse;

the outputs ~~output~~ of said first and second flip-flops are connected ~~coupled~~ to first and second inputs of a second multiplexer;

the control input of said second multiplexer is connected ~~coupled~~ to the output of an edge select register; and

the output of said second multiplexer is connected ~~coupled~~ to said output port.

Claim 3. (original) The state machine input/output circuit of Claim 1, further comprising a plurality of said input/output circuits, for providing data to a plurality of output ports, wherein said output ports are connected on an output data bus.

Claim 4. (canceled)

Claim 5. (currently amended) A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for passing data from an input port to a sampled output port, comprising:

a clock edge selector circuit having an input connected ~~coupled~~ to said input port and having an output, for selecting, in response to an edge select signal, data on said input port for provision to said selector circuit output selectably on either said rising edges or said falling edges of said clock signal;

a first multiplexer having a multiplexer ~~an~~ output connected ~~coupled~~ to a first flip/flop, said multiplexer having two inputs, a first one of said inputs receiving said selector circuit output, and a second one of said inputs connected ~~coupled~~ to the output of said first flip/flop and to the sampled output port, and

having a control input for selecting, in response to a control signal, said first input or said second input for connection to said first multiplexer output;

a control signal generator connected to a second multiplexer for generating a control signal to control said ~~a~~ second multiplexer to select said second multiplexer inputs for connection to said second multiplexer output;

a memory having a plurality of storage elements, each storage element being adapted to store a bit and provide the bit at a memory output of said memory ~~having an input and an output, said input being programmably connectable to either a state machine, microprocessor, or other programmably controllable data source for selection of data for storage therein~~, said memory outputs being connected to the inputs of said second multiplexer, wherein the output of said second multiplexer selects said first input or said second input of said first multiplexer for connection to said first multiplexer output.

Claim 6. (currently amended) The state machine input/output circuit of Claim 5, wherein ~~said clock edge selector circuit further comprises~~:

an input to said clock edge selector circuit is connected ~~coupled~~ to the input of a second and a third flip-flop being clocked at said state machine clock rate, said second flip-flop changing states on said rising edge of clock and said third flip-flop changing states on said falling edge of clock;

the outputs ~~output~~ of said second and third flip-flops are connected ~~coupled~~ to first and second inputs of a third multiplexer;

the control input of said third multiplexer is connected ~~coupled~~ to the output of a edge select register; and

the output of said third multiplexer is connected ~~coupled~~ to said output of said clock edge selector circuit.

Claim 7. (currently amended) The state machine input/output circuit of Claim 5, further comprising a plurality of said input/output circuits, for passing data from an input port to a sampled output port, wherein said input port is ~~inputs are~~ connected to ~~on~~ an input data bus and said sampled output port is ~~outputs are~~ connected to ~~on~~ an output bus.

Claim 8 (canceled)

Claim 9. (currently amended) A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for passing output data to an output port, comprising:

a memory having a plurality of storage elements, each storage element being capable of storing a bit and providing the bit as an output of said memory ~~having an input and an output, said input being programmably connectable to either a state machine, microprocessor, or other programmably controllable data source for selection of data for storage therein~~;

a first multiplexer having an output, having a plurality of inputs receiving the outputs of said memory, and having a control input for selecting, in response to a control signal, an input for connection to said output;

a control signal generator connected to said first multiplexer for generating a control signal to control said first multiplexer to select cyclically said first multiplexer inputs for connection to said first multiplexer output;

a second multiplexer having a first input and a second input, having an output, and having a control input for selecting, in response to a control signal, an input for connection to said second multiplexer output, said first input being connected ~~coupled~~ to a predetermined output data source, said output being connected ~~coupled~~ to a data ~~the control~~ input of a first flip-flop being clocked at said state machine clock rate, said second input being connected ~~coupled~~ to an

~~the~~ output of said first flip-flop and to the input of a clock edge selector circuit, and said control input being connected to said output of said first multiplexer;

said clock edge selector circuit connected to said second multiplexer for providing, in response to an edge select signal, the output of said second multiplexer to said output port selectably on either said rising edges or said falling edges of said clock signal.

Claim 10. (currently amended) The state machine input/output circuit of Claim 9, wherein ~~said clock edge selector circuit further comprises~~:

the inputs ~~input~~ of said second and third flip-flops are connected ~~coupled~~ to the output of said second multiplexer, said second flip-flop changing states on said rising edge of clock pulse and said third flip-flop changing states on said falling edge of clock pulse;

the outputs ~~output~~ of said second and third flip-flops are connected ~~coupled~~ to first and second inputs of a third multiplexer;

the control input of said third multiplexer is connected ~~coupled~~ to the output of an ~~a~~ edge select register; and

the output of said third multiplexer is connected ~~coupled~~ to said output port.

Claim 11. (currently amended) The state machine input/output circuit of Claim 9, further comprising a plurality of said input/output circuits, for passing output data to an output port, wherein said ~~output data is connected to on an input bus and said~~ output port ~~data~~ is connected to ~~on~~ an output bus.

Claim 12. (canceled)